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Description

METHOD FOR ESTABLISHING A GRAY CODE AND RELATED COUNTER CIRCUIT

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a method for establishing a Gray code, and more specifically, to a method for establishing a Gray code count sequence capable of counting any number of elements and a counter circuit related to the method.

[0003] 2. Description of the Prior Art

[0004] Binary countersarea common circuit elementrequired in digital systems such as personal computers or programmable controllers. Generally speaking, a binary counter counts numbers in a binary manner (e.g. 0000->0001->0010->0011->0100->...etc.). However, when a counter value switches to a next counter value, over one bit may need to change simultaneously. For in-

stance, from 0001 to 0010, the least significant bit changes from 0 to 1 and the second least significant bit changes from 1 to 0. When multiple bits changesimultaneously, a transient value such as 0011 may cause a glitch in the output of the binary counter so that a circuit using the output of the binary counter may not work normally.

[0005] In order to solve the problem mentioned above, a Gray code counter is used for counting. The Gray code counter counts numbers in a Gray code count sequence. Please refer to Fig.1 showing a list of decimal numbers 0-15 listed in sequence andtheir corresponding four-bit binary Gray code values. Using the Gray code count sequence, only one bit changes when switching from a counter value to the next counter value, and the last code word returns to the first code word by only changing one bit. This is referred to as the property of Gray codesthroughout the following description. In this manner, Gray codes solve the problem mentioned above. In Fig.1, the bit switch sequence indicates which bit changes when switching from the current counter value to the next counter value. If this sequence is regarded as an ordered set, in any ordered sub-set of the set, there willbe at least one number whichappears an odd number of times. This is referred to

as the property of the bit switching sequence throughout the following description.

[0006] However, conventional methods can only establish Gray code count sequences for 2^M elements, wherein M is the number of bits of eachcounter value, also referred to as a code word. A sequence for more than or less than 2^M elements but not havinga glitch in output of the counter circuit is impossible in the prior art. In other words, when the last element returns to the first element, there is still over one bit that needs to be changed.

SUMMARY OF INVENTION

[0007] It is therefore a primary objective of the present invention to provide a method for establishing a Gray code count sequence capable of counting any number of elements and a counter circuit related to the method.

[0008] Briefly summarized, a method for establishing a Gray code count sequence is disclosed. The method for establishing a Gray code count sequence having N code words includes determining a first bit switch sequence having 2^M-1 elements and the property of the bit switching sequence according to a first Gray code count sequence having 2^M code words, wherein 2^M is larger than N; determining a second bit switch sequence having N-1 elements and the

property of the bit switching sequence according to the first bit switch sequence; and determining a second Gray code count sequence according to the second bit switch sequence.

[0009] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of Drawings

[0010] Fig.1 is a list of decimal numbers 0-15 and the corresponding four-bit binary Gray code count sequence.

[0011] Fig.2 is a flowchart of a method to establish a Gray code count sequence according to the present invention.

[0012] Fig.3 illustrates the first Gray code count sequence according to the first embodiment of the present invention.

[0013] Fig.4 illustrates the second Gray code count sequence according to the first embodiment of the present invention.

[0014] Fig.5 illustrates the third Gray code count sequence according to the second embodiment of the present invention.

[0015] Fig.6 is a circuit diagram of a first bit unit in a counter according to the present invention.

[0016] Fig.7 is a circuit diagram of a second bit unit in a counter according to the present invention.

[0017] Fig.8 is a circuit diagram of a Gray code counter formed using the first bit unit in Fig.6 and the second bit unit in Fig.7.

DETAILED DESCRIPTION

[0018] Please refer to Fig.2 showing a flowchart of a method to establish a Gray code count sequence according to the present invention. The present invention provides a method to establish a Gray code count sequence having N elements and is described as follows:

[0019] Step10: Determine an exponent M according to N,such that 2^Misthe smallest integer that is larger than or equal to N.

[0020] Step12: Establish a first Gray code count sequence having 2^M elements.

[0021] Step14: Establish a first bit switch sequence having 2^M-1 elements according to the first Gray code count sequence. Each value in the bit switch sequence indicates the bit changes when an element changes to the next element.

[0022] Step16: Delete a proper number of elements from the first bit switch sequence to obtain a second bit switch sequence having N-1 elements.

[0023] Step18: Establish a second Gray code count sequence having N elements according to the second switch sequence.

[0024] As an example,consider establishing a Gray code count sequence having 6 elements. First, since N=6 define M=3.In other words, it is required to establish a first 3-bit binary Gray code count sequence having 2^3=8 elements, and establish a first bit switch sequence having 7 elements, as shown in Fig.3.

[0025] Then, delete some numbers from the first bit switch sequence to obtain a second bit switch sequence. In this embodiment, since only 6 code words are needed, it is required to delete 2 elements from the first bit switch sequence. Here the elements to be deleted are of the same value. Furthermore, please notice that in the second bit switch sequence obtained after deleting the 2 elements, it is required to maintainthe property that in any ordered sub-set of the sequence set, there is at least one number that appears an odd number of times. In case of the conventional Gray code bit switch sequence, there is a first element which is the middle number of the sequence and which can divide the whole sequence into a first ordered sub-set and a second ordered sub-set which are the

same. Take the first bit switch sequence {1, 2, 1, 3, 1, 2, 1} in Fig.3 as an example.The fourth element "3" is the middle number, by which the whole sequence is divided into two ordered sub-sets {1, 2, 1} which are the same. In the case of this embodiment, if the number of elements to be deleted is even, delete the same element in the same position and the same number from the first ordered sub-set and the second ordered sub-set respectively. From Fig.3, 2 elements are needed to be deleted, thus the first element "1" of the first ordered sub-set {1, 2, 1} and the first element "1" of the second ordered sub-set {1, 2, 1} are deleted. Please notice that, if element "2"were deleted, both the first ordered sub-set and the second ordered sub-set would have two elements "1" remaining.That does not comply with the bit switch sequence property, thus the deletion of element "2" is not allowed. The second bit switch sequence after deleting the two elements "1" is shown in Fig.4. Selecting elements to delete as above is only one of the embodiments of the present invention, any method that makes the second bit switch sequence comply with the bit switch sequence property also belongs to the present invention.E.g. delete mirrored symmetrical elements such as deleting the first element "1" of the first

ordered subset and the last element "1" of the second ordered subset.

[0026] In Step18, generate a 3-bit binary second Gray code count sequence having 6 elements according to the second bit switch sequence as shown in Fig.4. For example, the first number of the second bit switch sequence is 2, which means to toggle the second bit of the first element 000 in the second Gray code count sequence to obtain the second element 010. As shown in Fig.4, the second bit switch sequence also complies with the bit switch sequence property mentioned above, so that the probability of glitchesis reduced to the minimum.

[0027] Please refer to Fig.5 showing the second embodiment of the present invention. In the case of establishing a Gray code count sequence having 11 elements, proceed through Step10, Step12, and Step14 as mentioned in the first embodiment. As the relating details are the same to that of the first embodiment, a further description is hereby omitted. A first bit switch sequence obtained after finishing Step14 is shown in Fig.1.

[0028] In this embodiment, it is required to delete 5 elements from the first bit switch sequence to form a second bit switch sequence. In the case that the number of elements

to be deleted is odd, e.g. 5, firstly delete 4 elements from the first bit switch sequence in the same manner as in the first embodiment.Then delete one more element to obtain the second bit switch sequence. Please notice that in the second embodiment, when selecting elements whose number is even (in the same manner as in the first embodiment), the first element "1" of the first ordered subset and the last element "1" of the second ordered subset are first deleted. Additionally, when selecting the remaining element to be deleted, it is still required to have the second bit switch sequence comply with the bit switch sequence property. For example, firstly delete the first and the second element {1, 2} of a first ordered sub-set {1, 2, 1, 3, 1, 2, 1}, and the last two elements {2, 1} from a second ordered sub-set {1, 2, 1, 3, 1, 2, 1}. These two ordered sub-sets are divided by the element "4" being the middle number of the sequence. Then delete the third element "1" of the first ordered sub-set to obtain the second bit switch sequence shown in Fig.5.

[0029] By establishing the second Gray code count sequence in Fig.5 according to the second bit switch sequence, the goal of being required to toggle only one bit per each increment can be achieved. However, in the second Gray

code count sequence, two bits are changed when the last element 1001 returns to the first element 0000, thus when the last element 1001 returns to the first element 0000, the possible transient values are 1000 and 0001. In the first bit switch sequence an even plurality of elements are deleted,specifically, the first element of the first ordered sub-set and the last element of the second ordered sub-set are deleted.Thus the second Gray code count sequence does not include 1000 and 0001 so that a glitch cannot occur.

[0030] Please refer to Fig.6 showing a circuit diagram of a first bit unit 20 in a counter applying the Gray code count sequence according to the present invention, and to Fig.7 showing a second bit unit 30 in the counter. The first bit unit 20 in Fig.6 includes a first input Fi, a second input Zi, a clock input Clock, a reset input Rbar, a first output Fo, a second output Zo, and a bit output G. The first bit unit 20 further includes an XOR logic gate 22, a D flip flop 24, an AND logic gate 26, and an OR logic gate 28. The D flip flop 24 is reset to an output signal of 0 according to an active low reset input Rbar. Additionally, one of the input ends of the AND logic gate 26 is inverted. The interconnection between these devices is shown in Fig.6.

[0031] The difference between the second bit unit 30 in Fig.7 and the first bit unit 20 in Fig.6 is that the second bit unit 30 has a feedback input H, which is coupled with an input Q of the D flip flop via an XOR logic gate 40. The output signals of the XOR logic gate 40 are transmitted to an AND logic gate 36 and an OR logic gate 38 respectively.

[0032] Please refer to Fig.8 showing a circuit diagram of a Gray code counter formed using the first bit unit 20 in Fig.6 and the second bit unit 30 in Fig.7 according to the present invention. The counter 50 has three output signals (G2, G1, G0) representing three bits of the second Gray code count sequence respectively. When establishing the second bit switch sequence, element "1" is deleted an odd number of times (e.g. once) in the first ordered sub-set and the second ordered sub-setrespectively, thus the second bit unit 30 is used to output the first bit G0. Other elements such as "2" and "3" in the first ordered sub-set and the second ordered sub-set are not deleted, or are deleted an even number of times.Thus the first bit unit 20 is used to output the second and the third bit. The Gray code counter according to the present invention is composed of a plurality of first bit units 20 and a plurality of second bit units 30 connected serially.

[0033] Those skilled in the art will readily observe that numerous modifications and alterations of the method and device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.